Design and analysis of high performance Arithmetic and Logic unit for RISC processor in 32nm CMOS Technology

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Abstract— The advancements taking place in this modern epoch of digital world looks forward to optimize the available technologies to bring about efficient architectures that pave way for greater transformation in the field of electronics. In correspondence to the above issue, this paper portrays the low power technique used in an arithmetic and logic unit found in digital RISC processors to show high performance. Since there is large power dissipation taking place due to the internal operation of an arithmetic and logic unit, this paper aims to apply modified low power techniques at the transistor level to the processor simulated using HSPICE tool. Hence a new technique to design the control unit is provided to the processor to activate the internal components depending upon the requirement. This way the new architecture in 32nm CMOS technology performs it's processing with high speed thereby enhancing the processors' speed by cutting down the average power consumed along with the leakage power.

Index Terms— Low power, HSPICE tool, CMOS Technology, Optimization.

1 INTRODUCTION

In VLSI design methodologies power minimization is one of the primary concerns because a long battery life is required for mobiles and portable devices, Power dissipation is increasing due increasing rate of transistors on a single chip. Very Large Scale Integrated circuit technology is a rapidly growing technology for a wide range of innovative devices and systems that have changed the world today. With large integration density and improved speed of operation, systems with high frequencies are emerging [1]. Arithmetic Logic Unit (ALU) forms one of the core parts of a processor design. From program counter update to the address calculation of a jump instruction, ALU plays the major role. Current lower technologies at 130 nm raise several challenges in the circuit design. Power and performance have become head to head trade-off for the highly efficient designs. Several architectures of arithmetic circuits and ALU have been proposed in the past decade [10]. ALU is a combinational circuit that performs arithmetic and logical micro-operations on a pair of n bit operands [4]. Pseudo-nMOS logic is an example of ratio-ed logic which uses a grounded pMOS load and an nMOS pull-down network that realizes the logic function [6].In this logic the high output voltage for any gate is Vdd and the low output voltage is not 0volt. This results in decreased noise margin. The main drawback of this logic is very high static power consumption as there exists a direct path between Vdd and ground through the pMOS transistor shown in Fig 1.1.

Dynamic logic is well suited for high speed circuit design and requires less number of transistors, but the major drawback with this logic is, its excessive power dissipation due to the switching activity and clock.

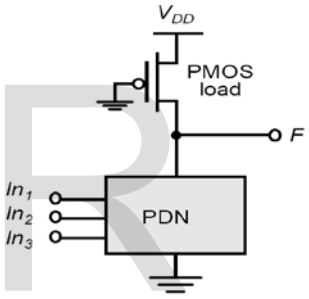

Fig 1.1 Pseudo nMOS Logic

Circuits having long logic depth need to have better speed and low power dissipation for which a new logic family called feed through logic are proposed in [5]. Here the above mentioned concept is extended to design the arithmetic and logic circuits. To ease the description and simulation, HSPICE simulating tool is widely adopted and it has numerous capabilities that are suited for designs of this sort. It provides transitory record of the system and allows the use of specific width to length ratios to cover the different abstraction criteria.

2 RELATED WORKS

The existing basic design consists of a conventional type of arithmetic and logic circuits that perform various arithmetic and logic operations required shown in Fig 2.1. When the architecture is simulated, it is found to consume more power due to the processing of all the elements [11]. The execution of all the blocks together adds up to high power dissipation with increased delay in processing. This was the main disadvantage from this design.

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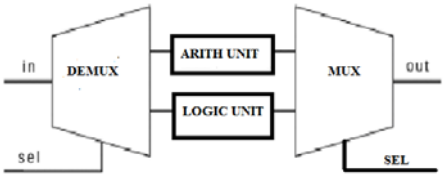

Fig 2.1 Basic Concept of ALU design

The basic ALU generates coded outputs depending upon inputs from general purpose registers [12]. These codes are used to indicate cases such as carry-in or carryout, overflow, divide-by-zero, etc. The step-wise design approach is essentially the breaking down of a system which defines the sub-systems present. Each subsystem is then refined in detail, sometimes in many additional subsystem levels, until the entire specification is reduced to base elements.

The existing feed through Logic, given in Fig 2.2, works in two phases, Reset phase and Evaluation phase [8], [9]. It can be shown, when clock input is high, the output node is pulled to zero value because transistor Tr is active and transistor TP is inactive. When clock goes low, reset transistor Tr is turned inactive and Tp becomes active resulting in charging or discharging of output node with respect to input. This creates an environment for leakage power to exist.

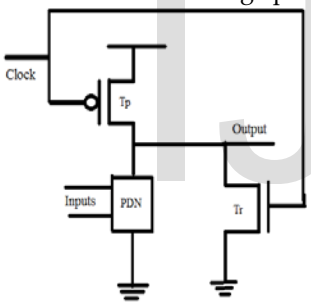

Fig 2.2 Existing Feed through Logic

3 Experiment and Design

This paper is divided into three distinct sections: modified low power technique needed to design the required control unit, an ALU designed using the low power technique and a RISC processor using both the above to function efficiently. The sections below are correlated to show the functionality.

3.1 Guarded Static CMOS logic

This section describes the power reduction technique used in the arithmetic and logic unit proposed. Here the guarded circuit controls the operation of the whole circuit designed with static CMOS logic. Hence the supply voltage is passed only when it is necessary. This proposed low power technique for ALU brings about greater accuracy and low complexity in the circuit design shown in Fig 3.1. This achieves high performance in terms of required use of supply voltage.

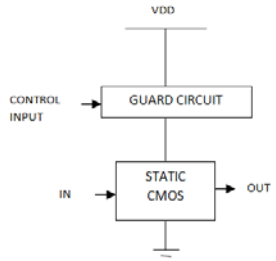

Fig 3.1 Guarded static CMOS logic

3.2 Proposed Arithmetic and Logic Unit

This section contains a precise discussion on the proposed arithmetic and logic circuit that is shown below in Fig 3.2 The proposed guard circuit logic from the previous section is incorporated in this arithmetic and logic unit design. Hence an additional loss in power consumption of the circuit is further observed. According to the block diagram below, each block is fed with two control signals. One of the control signals chooses whether the operation to be executed is arithmetic block or logic block. Hence the choice is made by the user in providing the arithmetic and logic unit with the necessary control input.

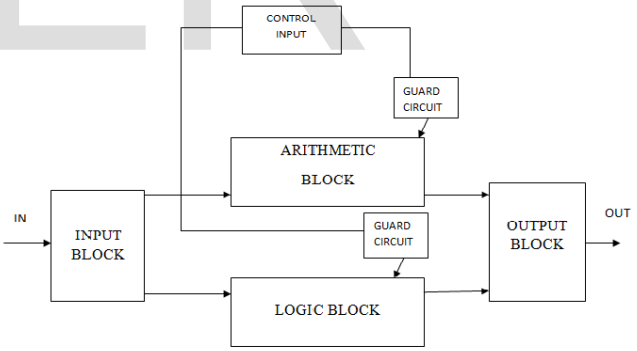

Fig 3.2 Modified Architecture of Arithmetic

3.3 RISC Processor with a Control unit

The explanatory architecture of the RISC processor is shown in Fig 3.3 below. This architecture consists of arithmetic logic unit, control unit, shifter (universal shift register) and rotator (barrel shifter). The processor is designed load/store Von Neumann architecture that exhibits shared memory and bus architecture for instructions and data transfer between processor and memory. Instruction in the form of digital bits is fetched in a sequential fashion so that the incurring latency can be reduced between the cycles of execution. Pipelining stages of are incorporated in the design which in turn

increases the speed of operation. RISC Processor works on reduced number of Instructions and fixed instruction length.

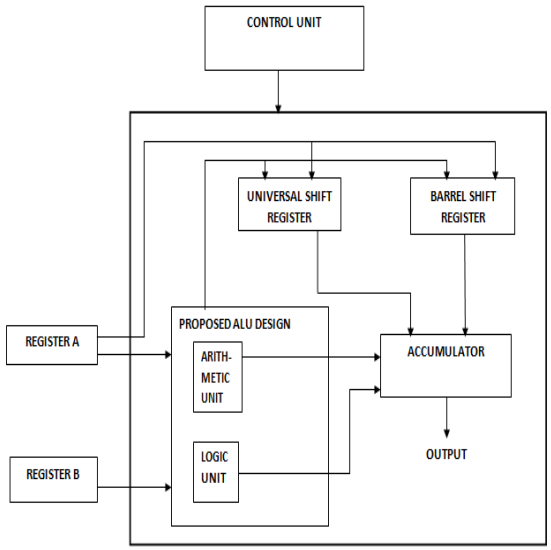

Fig 3.3 Modified Architecture of RISC processor

4 Results and Discussion

4.1 Transient Analysis

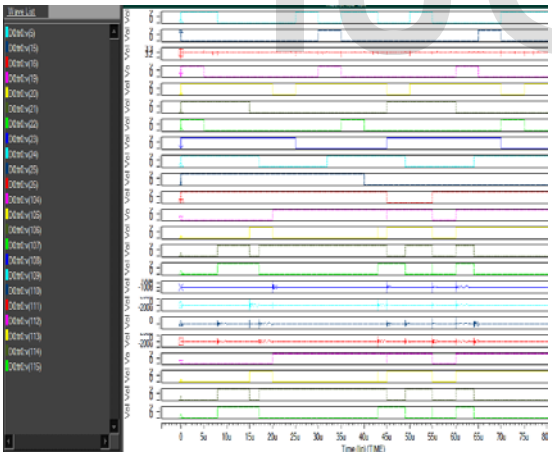

Fig 4.1 Transient analysis of proposed arithmetic and logic unit in 32nm CMOS technology

Fig 4.1 shows the output waveform of proposed technique for 32nm CMOS technology in which v(5), v(15), v(16) represents the ALU control input, v(19)-v(26) represents the ALU input, v(104)-v(107) represents the arithmetic unit output, v(108)-v(111) represents the logic unit output, v(112)-v(115) represents the ALU output.

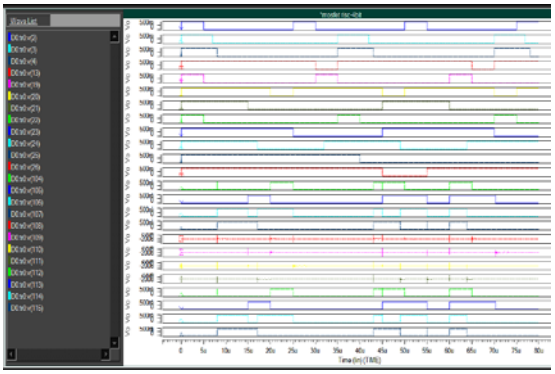

Fig.4.2 Transient analysis of proposed RISC processor in 32 nm CMOS technology

Fig 4.2 shows the output waveform of proposed technique for 32nm in which v(2)-v(4), v(13),v(14), v(19)-v(26) represents the RISC processor input, v(104)-v(107) represents the arithmetic unit output, v(108)-v(111) represents the logic unit output , v(112)-v(115) represents the RISC processor output.

4.1 Power Analysis

TABLE 1
POWER ANALYSIS OF EXISTING SYSTEM AND PROPOSED SYSTEM

DEVICE:MOSFET TECHNOLOGY:32nm OPERATING FREQUENCY:1GHz						
DESIGN	EXISTING			PROPOSED		
	Avg pwr (µw)	Delay (µs)	PDP (pJ)	Avg pwr (µw)	Delay (µs)	PDP (pJ)
ALU DESIGN	3967	0.125	495.8	11.94	1.001	11.95
RISC PROCESSOR	1886	7.854	14812	234.04	1.001	234.27

The above Table 4.1 shows the performance analysis report existing and modified arithmetic and logic circuit and the RISC processor in analysed in 32nm CMOS technology.

5 CONCLUSION

Thus the power consumption is greatly reduced in the modified design using the new guarded static CMOS logic and it is found to be more efficient. With the conventional type of arithmetic and logic unit that executes all the operations at the same time, the power dissipation gets uncontrolled. Hence to discover an alternative, the feed through logic was taken as a base and a proposed logic was introduced. The performance analysis clearly shows that the proposed arithmetic and logic unit used in the RISC processor gives appropriate dimensions of various parameters helping to obtain a near optimum circuitry. The proposed technique and designs can be used in high end real time applications like ARM processors, embedded processor, filter circuits and also in various other low power applications.

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